

Y. Kadowaki, M. Nakatani, T. Ishii, S. Mitsui and K. Shirahata
Semiconductor Laboratory, Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, Hyogo 664, Japan

ABSTRACT

A simple and convenient method on the design of GaAs MESFET power amplifiers are presented. Based on this method are constructed five-stage MIC amplifiers, which deliver 1 W power outputs at the 12 GHz band. Further brush-up of the power performance is investigated using newly developed flip-chip power MESFETs, resulting in 2 W power output.

Introduction

With the recent advancement of GaAs MESFET device technology, high power MESFET amplifiers have been developed in the 12 GHz band frequencies. For the design of the MESFET amplifier in this frequency range, FET chips are often used in order to minimize parasitics and obtain superior performances. In this work, however, packaged FETs are used from the standpoint of reliability, reproducibility and feasibility of design.

This paper describes (1) a simple and useful method on the design of power FET amplifiers, (2) a 12 GHz 1 W five-stage amplifier constructed with commercially available packaged FETs in house and (3) further brush-up of the power performance of the amplifier using newly developed flip-chip power MESFETs.

A Design Technique

For the design of high power MESFET amplifiers, output impedance S_{22} of the MESFET varies significantly with power levels and some design method optimizing output matching circuit is necessary.¹ However, the method is complicated compared to the design procedure for small signal amplifiers.

The design method used throughout this work is as follows. The change of S_{22} with the increase in power levels could be analyzed as a result of increases in drain conductance g_d and drain-gate feedback capacitance c_{dg} in the well-known small signal equivalent circuit model of the MESFET.² From this analysis could intuitively be considered that the spreading of the gate depletion layer, on average, under large signal operation would be analogous to that under small signal operation in an unsaturated condition. In order to ascertain the similarity, dependence of S_{22} on power levels, measured at 12.1 GHz by the Standing Wave Ratio Method, is compared, in Fig. 1, to that of small signal S_{22} , measured with an ordinary network analyzer, on drain bias conditions, resulting in some analogy.

On the basis of the result obtained in Fig. 1, 1 W power unit amplifier was so designed that the output circuit might be matched at 12 GHz under small signal operation at the drain bias of 2 V. The output power characteristics of the amplifiers are depicted in Fig. 2 together with the performance of an amplifier, with the same MESFET, designed under small signal output matching condition at the drain bias of 8 V, the operation bias of the MESFET.

Thus obtained output power was found nearly equal to the highest one independently delivered by retuning the circuit and the usefulness of this design method was proved.

A 12 GHz 1 W Amplifier

Configuration

The amplifier is composed of five unit amplifier modules. An inner view of the amplifier is shown in Fig. 3.

As shown in the block diagram of Fig. 4, three kinds of MESFETs (TYPE I, II, III) and two types of unit amplifier modules (single-ended and balanced) were used in this amplifier. The first stage is a balanced module using small signal TYPE I MESFETs and 90° interdigitated couplers³ for low noise preamplification.

The second stage is a single-ended driver composed of a medium power TYPE II MESFET. The third and the fourth stages are balanced modules of TYPE II MESFETs for medium power amplification. The performances of these medium power amplifier modules are the linear gain of 7.9 dB and 6.0 dB, the power output of 200 mW and 400 mW at 1 dB gain compression and the power added efficiency of 23 % and 18 % for a single-ended and balanced modules, respectively. The final stage is a single-ended module using a high power TYPE III MESFET. This high power module provides the linear gain of 3 dB and the power output of 1.1 W at 1 dB gain compression.

Performance

The overall characteristics at 12 GHz obtained for the completed five-stage amplifier are the linear gain of 27 dB and the power output of 0.8 W at 1 dB gain compression. The power output of 1 W was obtained with 24 dB gain.

Fig. 5 shows the frequency response of the amplifier at various input power levels. Each curve depicts the gain-bandwidth characteristic corresponding to the linear amplification range, the 1 dB gain compressed condition and the nearly saturated state. The 1 dB bandwidth at each input power level is 500 MHz, 450 MHz and 350 MHz, respectively.

Fig. 6 shows the third order intermodulation characteristic and AM/PM conversion performance. The intercept point is +40 dBm and the AM/PM conversion is -2.5°/dB at 1 dB gain compression point.

At the frequency of 12 GHz, noise figure was about 6 dB, and input/output VSWRs were lower than 2.5:1 for the linear amplification range.

Higher Power Output

Flip-chip power MESFET

Further brush-up of the power performances of the 1 W amplifier was investigated using newly developed flip-chip power MESFETs, MGF-2100 series. These FETs are fabricated by mounting all electrodes of the FET chip directly on the pedestals of the package. The structure with no bonding wires leads minimization of parasitics, especially, source inductance, resulting in the improvement of the gain-bandwidth characteristic as well as power performances. As a result, such performances as 5.5 W at 10 GHz, 4 W at 12 GHz, and 2.5 W at 15 GHz are obtained for packaged FETs.⁴

Unit amplifiers

With these flip-chip MESFETs, several unit amplifiers were fabricated for the 12 GHz band frequency. In Table 1 are summarized the linear gain G_L , the output power at 1 dB gain compression point P_{1dB} , the saturation power P_{sat} and the power added efficiency η_{add}

of these amplifiers. Fig. 7 shows, as an example, output performances for single-ended and balanced amplifiers with MESFETs of $W_g = 4800 \mu\text{m}$.

High output power of 4 W was obtained for the balanced type.

Five-stage amplifier

A five-stage amplifier was constructed using two of these flip-chip MESFETs. Configuration and performance of this amplifier are shown in Fig. 8 and Fig. 9, respectively. Linear gain of 29 dB was obtained with 1.2 W output power at 1 dB gain compression and with 2 W saturation power.

Conclusion

From this work, followings are concluded;

- (1) simple and useful method using small signal S_{22} at a shallow drain bias condition was presented on the design of power MESFET amplifiers.
- (2) a five-stage MIC amplifier was constructed with commercially available packaged FETs produced output power of 1 W with linear gain of 27 dB.
- (3) Further brush-up of the power performance of the amplifier was investigated using newly developed flip-chip power MESFETs. Saturated power of 4 W and 2 W were obtained for a unit and a five-stage amplifier, respectively.

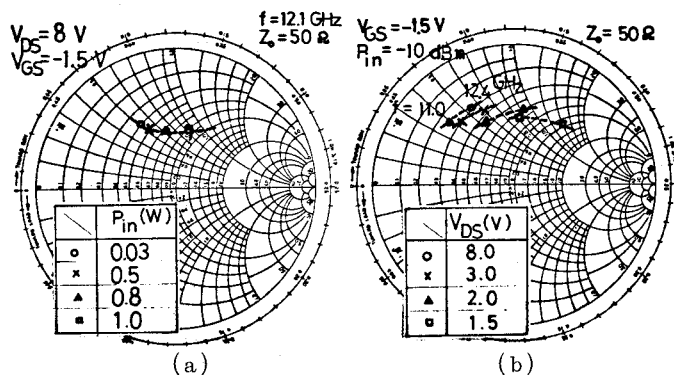


Fig. 1 Dependence of S_{22} on power level (a) and drain bias (b)

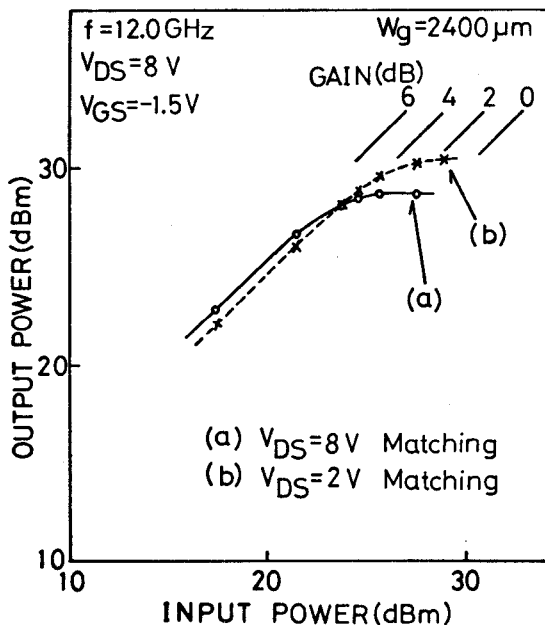


Fig. 2 Power output performances of designed amplifiers

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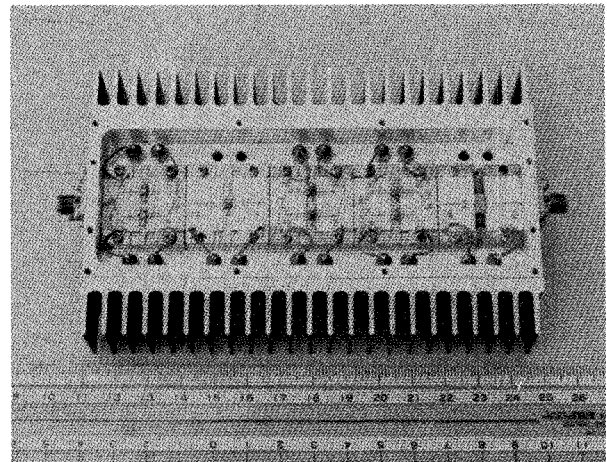


Fig. 3 Photograph of five-stage GaAs MESFET amplifier

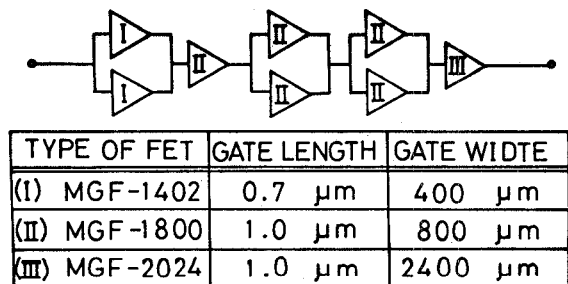


Fig. 4 Block diagram of five-stage GaAs MESFET amplifier

TYPE OF FET	GATE LENGTH	GATE WIDTE
(I) MGF-1402	0.7 μm	400 μm
(II) MGF-1800	1.0 μm	800 μm
(III) MGF-2024	1.0 μm	2400 μm

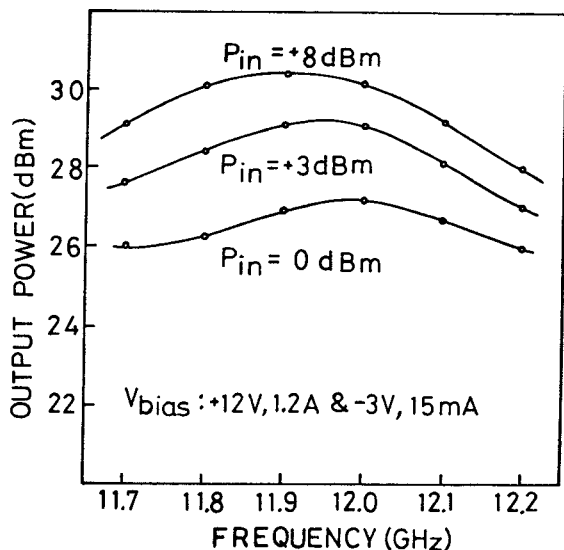


Fig. 5 Frequency response of five-stage GaAs MESFET amplifier

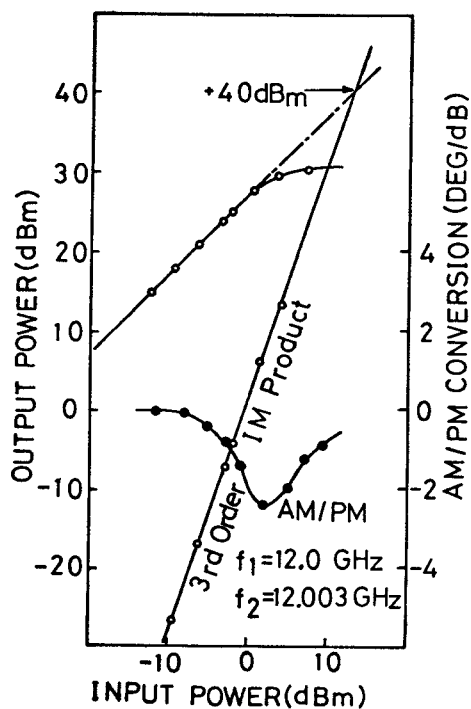


Fig. 6 Third order intermodulation characteristic and AM/PM conversion at 12 GHz for five-stage amplifier

Table 1 Principal characteristics of unit amplifier modules using flip-chip power MESFETs

W_g (μm)	G_L (dB)	P_{idB} (W)	P_{sat} (W)	η_{add} (%)
2400	5.2	0.93	1.2	18
2400 x 2	4.0	1.95	2.3	14
4800	4.0	2.3	2.6	18
4800 x 2	3.0	3.2	4.0	10

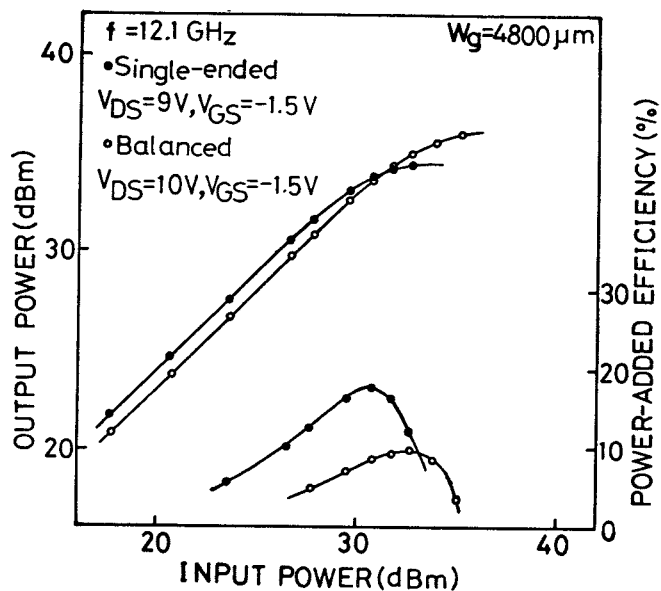
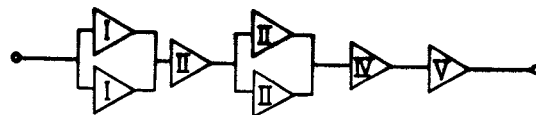


Fig. 7 Power output performances of unit amplifier module examples



TYPE OF FET	GATE LENGTH	GATE WIDTH
(I) MGF-1402	0.7 μm	400 μm
(II) MGF-1800	1.0 μm	800 μm
(IV) MGF-2124	1.0 μm	2400 μm
(V) MGF-2148	1.0 μm	4800 μm

Fig. 8 Block diagram of improved five-stage amplifier

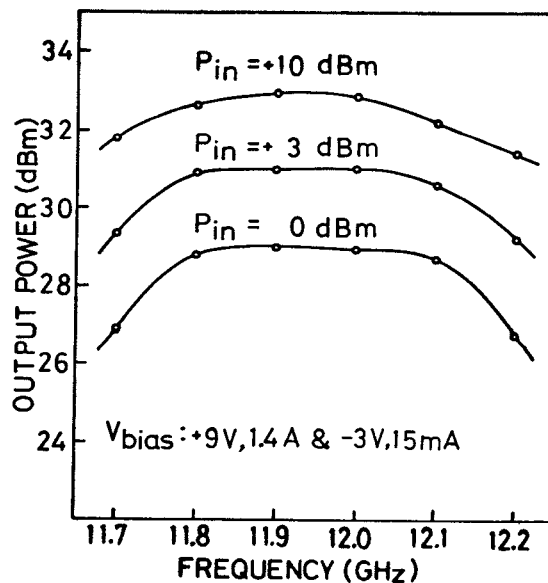


Fig. 9 Frequency response of improved five-stage amplifier